Listing and Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1   1. (original)   A method for sampling a digital signal yielding improved jitter
2   performance within prescribed bandwidth constraints, comprising the steps of:
3   periodically sampling the digital signal n times during every interval t, with n chosen such
4   that $\log_2(n+1)$ is an integer (x) greater than zero;
5   generating a $x+1$-bit sample value after each interval t, the sample value having a first bit
6   indicating the value of the digital signal being sampled, and x remaining bits which collectively
7   indicate a sample interval during which the digital signal changed states if such a change did
8   occur, and
9   inverting the first bit of each sample value upon decoding to coincide with the change in
10   the digital signal.

1   2. (original)   The method according to claim 1 wherein $n=15$ and x equals 4.

1   3. (original)   Apparatus for sampling a digital signal yielding improved jitter
2   performance within prescribed bandwidth constraints, comprising of:
3   a sample clock for generating n periodic clock pulses during every interval t, with n
4   chosen such that $\log_2(n+1)$ is an integer (x) greater than zero;
5   a receiver for generating a $x+1$-bit sample value after each interval t, the sample value
6   having a first bit indicating the value of the digital signal being sampled, and x remaining bits
7   which collectively indicate a sample interval during which the digital signal changed states if
8   such a change did occur, and the receiver inverting the first bit of each sample value upon
9   decoding to coincide with the change in the digital signal.

1   4. (original)   The apparatus according to claim 1 wherein $n=15$ and x equals 4.

1   5 (new)   A method for sampling a digital signal yielding improved jitter
2   performance within prescribed bandwidth constraints, comprising the steps of:
3   periodically sampling the digital signal n times during every interval t, with n chosen such
4   that $\log_2(n) =< x$ where x is an integer;

5   generating a $x+1$-bit sample value after each interval t, the sample value having a first bit

6   indicating the value of the digital signal being sampled, and x remaining bits which collectively

7   indicate a sample interval during which the digital signal changed states if such a change did

8   occur, and

9   inverting the first bit of each sample value upon decoding to coincide with the change in

10   the digital signal.

1   6. (new)   The method according to claim 5 wherein $n=15$ and x equals 4.

1   7. (new)   Apparatus for sampling a digital signal yielding improved jitter

2   performance within prescribed bandwidth constraints, comprising of:

3   a sample clock for generating n periodic clock pulses during every interval t, with n

4   chosen such that $\log_2(n) =< x$ where x is an integer

5   a receiver for generating a $x+1$-bit sample value after each interval t, the sample value

6   having a first bit indicating the value of the digital signal being sampled, and x remaining bits

7   which collectively indicate a sample interval during which the digital signal changed states if

8   such a change did occur, and the receiver inverting the first bit of each sample value upon

9   decoding to coincide with the change in the digital signal.

1   8. (new)   The apparatus according to claim 7 wherein $n=15$ and x equals 4.